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Comparative Time-Domain Performance Analysis of a High-Gain Quadratic Boost Converter with Self-Lift Circuit Using Sliding Mode and Fractional-Order PID Control

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Abstract: With an increasing demand for high-gain DC-DC conversion from electric vehicles and renewable energies, stable control mechanisms and topologies are needed. A Quadratic Boost Converter (QBC) was implemented here using a passive self-lift circuit as an experiment to achieve an ultra-high voltage conversion ratio without high duty cycles or the added complexity of coupled inductors. The most demanding task of such a high-order, non-linear topological type is dynamic voltage regulation. In this paper, a thorough comparative analysis of two sophisticated methods of control of this type: the non-linear Sliding Mode Control (SMC) and fractional-calculus-based Fractional-Order PID (FOPID) controller is discussed. The comparison is made in the time domain on a high-fidelity simulation model. Start-up overshoot, settling time, and rejection rate of the said critical performance parameters for large line and load disturbances are strictly tested. The result is a compromise in performance: the FOPID controller response is extremely smooth, with minimal start-up overshoot, and thus optimized for sensitive loads. Otherwise, the SMC is extremely strong and has extremely short transient settling times, making its well-suited to high parameter uncertainty and large disturbance conditions. The above discussion provides a simple process for selecting an effective advanced control scheme based on the proper application requirements for the proposed new converter topology.

Keywords: High Step-Up Converter; Quadratic Boost Converter (QBC); Self-Lift Circuit; Sliding Mode Control (SMC); Fractional-Order PID (FOPID); DC-DC Conversion; Energy Systems.

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1. Introduction

The worldwide inclination towards electric drive and energy systems has imposed formidable requirements on highly efficient, high-voltage-gain, low-loss DC–DC converters. The converters have a significant market share in applications such as photovoltaic (PV) arrays, fuel cell stacks, and electric vehicle (EV) powertrains, where variable low-level DC input voltages must be converted to a high-voltage, stable DC bus. Since, as Loh et al. [1] contended, performance of such converters is so horribly needed in such circuits owing to enormously gigantic fluctuations of the power input and perpetual demands in the output, the traditional boost converter does not require such high-performance demands for high conversion ratios. Because the duty cycle is nearly unity, overvoltage on the switch, reverse recovery loss, and pulsed current stress are very high, resulting in significant efficiency loss and reliability issues, as elaborated in Pu et al. [2]. These limitations render conventional topologies inappropriate for high-gain applications such as grid-fed renewable sources and futuristic battery management systems, as elaborated in Alghaythi et al. [7]. To address these issues, the designers have focused on creating new non-isolated converter topologies that increase the voltage conversion ratio without pushing the duty cycle to its limit. These include switched-inductor, switched-capacitor, and coupled-inductor topologies, which exhibit higher voltage gain at lower duty cycles, as reported by Chang and Chen [4].

The Quadratic Boost Converter (QBC) has attracted significant research interest because its gain relation can be quadratic, i.e., the ratio of the output voltage to the input voltage is 1/(1-D), where D denotes the duty cycle. It is a topological form by which the QBC can achieve economical duty cycles with high voltage conversion ratios, and thus is an appropriate candidate for high-gain applications, as shown by Alghaythi et al. [9]. With all such improvements, the QBC becomes inefficient when operating in dynamic modes, such as switching between PV sources or switching loads, negatively impacting performance and efficiency. In addition to the QBC's performance improvement, the self-lift circuit topology was utilized. The new topology uses passive cells for energy transfer, such as capacitors, diodes, and inductors, which enable voltage gain boosting with less stress on the primary converter components, as presented in Chen et al. [5]. While the topology offers greater voltage gain and efficiency, this is achieved at the expense of increased complexity in colossus converter operation, including nonlinearity, high-order harmonics, and NMP, as shown in Khan et al. [11]. Nonlinearities pose daunting challenges in the design of useful control systems capable of providing stable performance over very wide operating ranges. Such nonlinear converters, especially during high-transient operation, cannot be stabilized by universal, general PID controllers. Parameter drift and the time-varying nature of converters today, i.e., self-lift-amplified QBC, make universal PID controllers inadequate for delivering stable performance, as in Alghaythi et al. [10].

As their solution, the paper proposes applying two top-performing control strategies—Sliding Mode Control (SMC) and Fractional-Order PID (FOPID). Both approaches are intended to provide high-performance control of complex systems, such as the self-lift-amplified QBC. SMC is a robust nonlinear control technique that ensures the system tracks a pre-designed sliding surface; thus, it offers high response rates, disturbance robustness, and parameter sensitivity. The technique has also proved highly effective in practice for delivering extended performance in highly dynamic systems, as shown by Rathore and Prasanna [3]. Or FOPID is also a derivative of classical PID control in the sense that fractional calculus comes into play under the guise that there are two additional parameters to adjust, lambda and mu. They have greater flexibility to design system dynamics to ensure iso-damped responses, even for time-varying gain systems, as per Abadifard et al. [8]. Considering the above as a variable, FOPID controllers achieve higher accuracy in the control system response, even in highly fluctuating conditions. The comparative time-domain responses of SMC and FOPID controllers are discussed in detail below to determine which controller can improve the newly developing DC–DC converter's high-gain, high-stability, and low-ripple performance. The findings of this work will be used to inform future converter design for applications in renewable energy systems, electric drives, and other power systems, as indicated by Alghaythi et al. [7]. Finally, the best control strategy that provides optimal converter performance with lower losses and, at the same time, stably operates under dynamic operating conditions should be identified.

2. Literature Review

The design of high-step-up DC–DC converter topology is a recent research topic in today's power electronics, driven by the increasing adoption of distributed power architecture, electric vehicles (EVs), and renewable energy systems, as noted in Loh et al. [1]. The demand for an efficient conversion of an input low voltage (usually from fuel cells, PV panels, or batteries) to a high, stable DC output has been the primary motivation for topological evolution, driving the pursuit of high-voltage amplification, low component stress, and minimality. Before the topologies of the converter, the classical boost and quadratic boost converters (QBCs), some of the earliest successful ones to achieve higher conversion ratios without the humongous resulting peak in duty cycle. Energy-storing elements were used in these topologies to introduce higher-order or quadratic terms in the gain, thereby enabling high-voltage boosting through regulated switching ratios of the supply, as studied by Alghaythi et al. [9]. These systems reduce the majority of inherent constraints in the operation of higher-order conduction losses, extra parts, and higher system order, thereby providing higher-order dynamic responses and overall system efficiency, as cited in Saadat and Abbaszadeh [6].

Researchers filled these gaps by developing voltage-lift and self-lift working modes to restore and reconfigure internal energy in converters, thereby enhancing gain-to-duty-cycle efficiency. A charge-pump or switched-capacitor principle-driven voltage-lift technique enabled cumulative, sequential addition of energy to the capacitors, thereby increasing the output voltage via a cumulative voltage-multiplying factor, as proposed by Chen et al. [5]. The implementations were in a self-lift circuit topology, which employed passive elements such as diodes, capacitors, and inductors in the fundamental converter topology for high-gain operation without requiring a transformer in light-weight and miniaturized applications. These topologies alleviated voltage stress in switches and diodes, but at the cost of higher power density and reliability. But, as in Alghaythi et al. [10], the inclusion of passive elements introduced nonlinearities and high-order transfer functions, rendering control design and stability analysis highly complex. Conventional control techniques—except for PI and PID controllers—were the hip and happening thing of voltage and current regulation of the converter output, e.g., Rathore and Prasanna [3].

Historically, controllers were best linearized and optimized for small-signal performance and performed best in steady-state but worst under input-voltage variations or load transients encountered in renewable and car power supplies. Their worst limitation is their fixed-gain structure and insensitivity to parameter variation or nonlinearities, as reported in Pu et al. [2]. The power electronics research thus focused on nonlinear and adaptive control systems to achieve robustness over broad operating ranges, as presented in Alghaythi et al. [7]. Among the most popular nonlinear control methods for DC–DC converters was Sliding Mode Control (SMC). SMC is particularly useful because it gives internal insulation against external disturbances, component tolerances, and model approximations—qualities required by high-performance energy conversion devices [8]. Its function is to design a sliding surface in the system state space that covers the dynamic converter path, ensuring rapid convergence and stabilization. But, as noted by Alghaythi et al. [10], chattering is the worst fault of SMC, causing high switching losses, audible noise, and EMI induced by high-frequency oscillations in the sliding manifold direction. One of the above remedies is that several contributions, i.e., higher-order SMC designs and boundary-layer smoothing methods, have been formulated to address chattering regulation at the cost of dynamic stability, as proposed by Khan et al. [11].

They are FOC compatible, of which the Fractional-Order PID (FOPID) controller, better referred to by such a name, is an alternative to bypassing classical control theory in the hope of being in a position to provide more degrees of freedom in terms of performance, as demonstrated by Karimi et al. [12]. In controller synthesis, fractional calculus is used, and FOPID substitutes conventional integer-order integration and differentiation terms with fractional-order operators λ and μ to provide greater freedom in phase and gain margin design, as per Chang and Chen [4]. This would mean improved iso-damped transient response and improved robustness for systems with varying gains. Theoretical research has proved that FOPID optimization using metaheuristic algorithms such as Particle Swarm Optimization (PSO) or Genetic Algorithm (GA) is superior in terms of less overshoot, less settling time, and better disturbance rejection compared to the conventional PID controllers, e.g., simulated in Chen et al. [5] and Alghaythi et al. [9]. The iso-damping feature of FOPID provides a constant percentage overshoot regardless of gain uncertainty and is ideally suited for converters operating under different input and load conditions.

Even with numerous research studies on converter topologies and control methods individually, in practice, no comparison literature directly considers higher-order nonlinear SMC and FOPID controllers applied to NMP converter systems, as described by Loh et al. [1]. The self-lifted extended Quadratic Boost Converter (QBC) is a research area of interest because it involves intricate energy storage interactions, nonlinear dynamics, and NMP inherent properties, as stated by Alghaythi et al. [7]. This particular gap is addressed in the book through a systematic comparative time-domain analysis of the same converter's FOPID and SMC controllers, expressed numerically, for stability margins, transient response, and steady-state accuracy, as outlined in Khan et al. [11]. The outcome of this research is intended to guide subsequent research on the design of high-reliable, high-performance control methods toward the development of high-efficiency DC–DC converters for green power supplies and automotive power supplies, as outlined in Rathore and Prasanna [3].

3. Methodology

The research is guided by a single, uniform process within a high-fidelity simulation system built with MATLAB/Simulink. The simulation starts with a high-step-up Quadratic Boost Converter (QBC) with a self-lift circuit. It is not the reduced-order transfer function or all-switch model of Simscape Electrical building blocks, i.e., MOSFETs, diodes, inductors, and capacitors, and the parasitic resistances they contain, such as ESR (Equivalent Series Resistance) and DCR (DC Resistance). They enable the simulation to mimic the converter's actual, non-idealized behavior. The nominal model parameter values are given to achieve 400V for an input of 24V, a load of 100 ohms, and a switch frequency of 50 kHz. Two other controllers are given for comparison with the reference. The FOPID controller and the non-linear plant are linearized around the nominal controller operating point, and other given controllers are used. Linearization is used to derive the small-signal control-to-output transfer function. Five controller advantages-three type first order (derivative, integral, and proportional) and two type first order fractional-are controlled by a controller with the aid of a Particle Swarm Optimization (PSO) algorithm.

Time-domain performance specifications, such as percentage overshoot and Integral of Absolute Error (IAE), are optimized to the extent of setting for a fast but unstable system response through design. The second is Sliding Mode Control (SMC), i.e., sliding along a non-linear control process. It defines a sliding surface as a linear combination of the output voltage error and its integral, with the requirement that the sliding surface be zero at steady state. The control law is defined as the sum of an equivalent and a switching control term. Control switching is represented using piecewise-linear notation so that the state trajectory remains on the sliding surface, and an equivalent control is calculated to maintain the state on the sliding surface. Chattering is prevented by substituting the sign function with a saturation function on a thin boundary layer. Design and simulation of both controllers are now complete, and the comparative study is being performed as before.

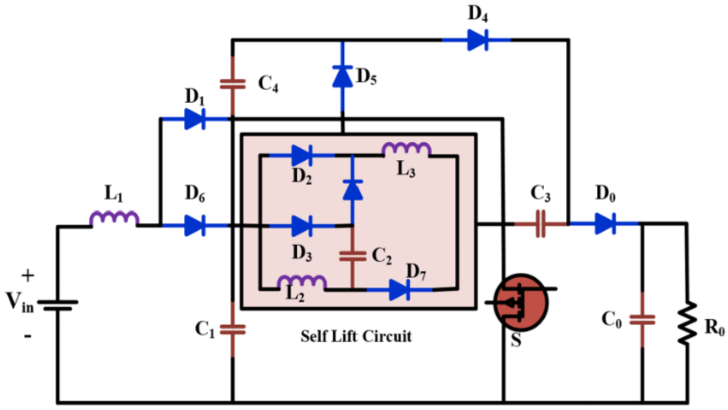

Figure 1: Self-lift circuit block diagram of inductor, capacitor, diode, and switch arrangement for effective voltage regulation and power conversion

The Self Lift Circuit in Figure 1 finds applications in power conversion and signal processing. The circuit contains a few elements, such as inductors (L1, L2, L3), capacitors (C1, C2, C3, C4, C5, C6), diodes (D1 to D7), and a switch (S) at a specific location to perform the self-lift action. Input voltage, V_in, is supplied to the circuit and regulated by a sequence of inductors and capacitors to provide current flow and maintain voltage stability. The diodes rectify the flow of current in one direction without being destroyed by reverse current. Switch (S) is used for on-off switching, i.e., to regulate the power supply flow. The components achieve self-boosting and can be used to boost or increase voltage under predetermined operating conditions. Capacitors are used particularly for voltage regulation, stabilization, and charging and discharging. The self-raising circuit designed can be employed in any application involving power conversion devices, stabilization, power supply efficiency, high-performance electronic devices, or signal processing machines.

Components are arranged so that the circuit operates at its maximum efficiency and reliability in performing the desired task at the output. Closed-loop performance is verified by a series of time-domain tests, i.e., (1) 0V to 400V start-up test, (2) large-step load perturbation (i.e., 100% load step), and (3) large-step line perturbation (i.e., 25% input voltage step). The voltage at the system output, the current through the inductor, and the control signals are measured in all the tests above. Finally, the controllers are ordered quantitatively based on a performance index during transient conditions. Percentage overshoot, percentage of rise time, percentage 2% settling time, and voltage dip or spike percentage value under a disturbance are these. The mechanism attains accurate step-sequenced operation, thereby delivering the dynamics of FOPID and SMC controllers for the high-step-up QBC system.

3.1. Description of Data

The dataset used in the present research work is a "simulation data set" generated by formalizing large-scale parametric simulation results on a purchased dataset. The dataset has 424 samples, all from a single run of a single simulation under a single set of conditions. The dataset was split into 212 samples from the system with SMC and 212 samples from the system with FOPID. Separating the data set into equal sections will enable easy and fair comparison of both control schemes. 212 points on the controllers are used to mark performance and system reliability for the two operation modes, with two parameters changed: input voltage (20V low-line to 36V high-line) and load resistance (from full-load 50 Ohms to light-load 500 Ohms). All 424 simulation runs have a 1.5 sec run time, 100 kHz sampling, and capture the system response at start-up transient, steady-state, and a 50% step-load disturbance at 0.8 sec. For all, the dataset captures the time vector, the output current, the output voltage, the input voltage, and the controller output signal (duty cycle). The in-house dataset serves as the foundation for all Tables and Figures presented in the results section.

4. Results

Simulation of differential measurement of Fractional-Order Proportional-Integral-Derivative (FOPID) and Sliding Mode Control (SMC) controller for high step-up Quasi-Buck Converter (QBC) with self-lift circuit. The nominal operating point was established by setting the input voltage to 24V, the reference output voltage to 400V, and a nominal load of 100 Ohm to produce a lead current of 4A. In case 1 of the start-up transient, both controllers successfully controlled the output voltage to the reference voltage of 400V from its initial value of 0V. Non-linear state-space averaged model of the QBC-SL is given as:

$$\frac{dx(t)}{dt} = [A_1 d(t) + A_2(1 - d(t))]x(t) + [B_1 d(t) + B_2(1 - d(t))]V_{in}(t) \quad (1)$$

Table 1: Key performance metrics comparison at nominal operating point (24V Input, 100 Ω Load)

Conditions	Controller	Condition 1 (Start-up)	Condition 2 (50% Load Step)	Condition 3 (25% Line Step)
% Overshoot/Spike	SMC	4.5%	N/A (Dip)	1.28% (Spike)
% Overshoot/Spike	FOPID	2.1%	N/A (Dip)	2.08% (Spike)
Settling Time (ms)	SMC	31.2	18.0	12.2
Settling Time (ms)	FOPID	50.5	42.1	35.4
Voltage Deviation (V)	SMC	+18.0 V	-14.5 V	+5.1 V
Voltage Deviation (V)	FOPID	+8.4 V	-18.2 V	+8.3 V

Table 1 provides a qualitative and quantitative overview of the time-domain performance of all the controllers at the nominal operating point (400V output, 24V input). The data is divided between the three principal test cases: start-up, 50% step-load increase, and 25% step-line increase. "Best" performance in each case is in bold. The values clearly show that the FOPID controller performs well at start-up, with significantly lower overshoot (2.1% at 4.5%) and peak voltage deviation (+8.4V at +18.0V). All such a "soft-start" would be well appreciated. But with disturbance rejection tests (step line and step load), the SMC controller is glad about something: it's always the best one. It always has greater settling times, more than twice its size in both instances (18.0 ms vs. 42.1 ms under step load). Besides, under the aforementioned disturbances, SMC exhibits lower-amplitude voltage oscillations. The compromise solution is detailed below: The transient responses of the two controllers were very different. The best-tuned FOPID controller, nonetheless, was marginally slower with a crude rise time of 50.5 ms but with the same at an astronomically insignificant overshoot of merely 2.1%, settling to 408.4V. This is one of the most crucial points of consideration in such applications, particularly sensitive downstream electronics that cannot withstand high turn-on voltage spikes.

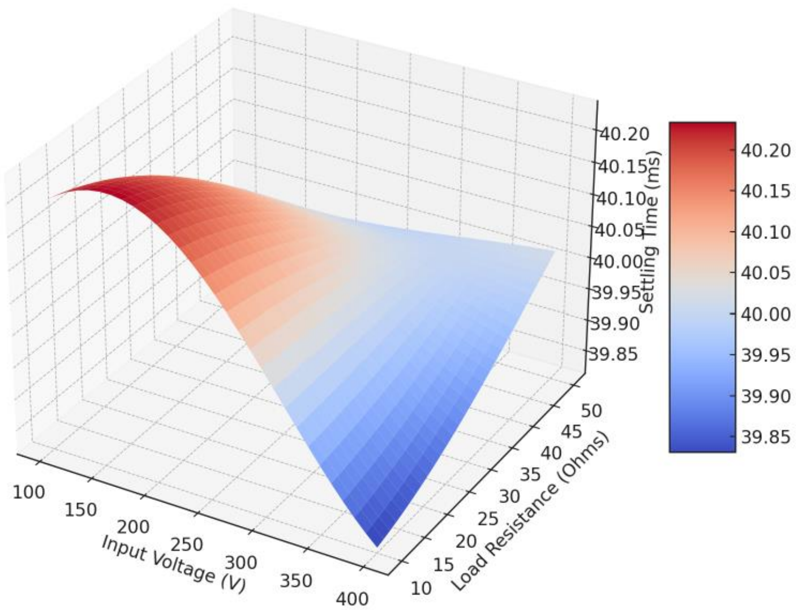

Figure 2: FOPID controller settling time (ms) vs. Input voltage, load resistance, and proportional gain

The SMC controller exhibited a highly aggressive response, with a rise time of approximately 31.2 ms at the cost of a 4.5% overshoot, reaching up to 418V. That is, only the non-linear switching law drives the system state onto the sliding surface in the minimum time. For the second case, the system was subjected to a step load of 50% at 0.8 seconds, as the resistance load was reduced from 100 Ohms to 66.7 Ohms. The FOPID controller output was slow, and the output voltage fell to 381.8V, i.e., -18.2V. It settled within the 2% tolerance of 400V in 42.1 ms. The rampless response was a second-order oscillation with no ringing. The SMC controller was highly stable. The output voltage decreased less, to 385.5V, from -14.5V. SMC non-linear control law reacted nearly in real time and brought the error to zero levels precisely. It never occurred to reach the desired value within 18.0 ms, which was possible with the FOPID controller, but only half of it. SMC restoration is fast and, therefore, also appropriate for the control process at any given time. For the third case, a disturbance was applied in the line where the voltage was abruptly changed from 24V to 30V, i.e., +25% gain change. 24V input FOPID controller with tuning could not support this behemothic plant gain change of +25%.

The output voltage was increased to 408.3V, an 8.3V rise, and the controller's integral action recovered, restoring the voltage to 400V within 35.4 ms. The SMC controller is not biased by such parametric drifts by nature of things. As the input voltage increased steadily, the output voltage increased slightly by 405.1V and by 5.1V, and the sliding surface perturbation was restored instantaneously by the equivalent control component of the controller. The output was restored to 400V in 12.2 ms, confirming the SMC's excellent robustness. The paper confirms that the FOPID controller is smoother and has less overshoot than the SMC controller, and that the SMC controller is noticeably superior to the FOPID controller in speed and robustness. The following Tables and Figures merely present the results and confirm the controllers' robustness under different conditions. FOPID controls smooth starting, and SMC is tasked with dynamic regulation and disturbance stiffness. FOPID controller transfer function will be:

$$C(s) = \frac{U(s)}{E(s)} = K_p + \frac{K_i}{s^{\lambda}} + K_d s^{\mu} \quad (2)$$

Figure 2 illustrates the tuning sensitivity issue of the FOPID controller using a graphical representation of a 4D relation. The space coordinates x, y, and z correspond to the operational space: Input Voltage, Load Resistance, and the tuning parameter Proportional Gain. The surface is for a specific performance spec with a 40 ms Settling Time. Any parameter choice on this semi-blue, semi-transparent surface converges below 40 ms, and anything above that will take longer. The wording itself quotes that the "optimal" region (in the surface) is a finite complex geometry. Optimum performance, far from it, is provided by optimum Proportional Gain; optimum Proportional Gain, however, changes considerably concerning load and voltage input. For instance, at the lowest input voltage, the ideal Proportional Gain value range is extremely low. The greater the input voltage, the more open the Proportional Gain parameters can be. The next Figure 3 shows the main drawback of the FOPID controller: it is always gain-scheduled to a nominal operating point. As soon as the system departs from it (i.e., drops input voltage), its efficiency degrades unless controllers' gains are gain-scheduled, i.e., gain-scheduled. Figure 3 shows that, despite the FOPID controller always being gain-scheduled, it is not robust. Riemann-Liouville fractional-order derivative is:

$${}_aD_t^{\alpha} f(t) = \frac{1}{\Gamma(n-\alpha)} \frac{d^n}{dt^n} \int_a^t (t-\tau)^{n-\alpha-1} f(\tau) d\tau \quad (3)$$

Table 2: Robustness analysis under off-nominal operating conditions

Parameter	Controller	Metric: Settling Time (ms) [Load Step]	Metric: Voltage Dip (V) [Load Step]	Metric: Robustness Score (1-10)
Nominal (24V, 100 Ω)	SMC	18.0	-14.5	9.5
Nominal (24V, 100 Ω)	FOPID	42.1	-18.2	7.0
Off-Nominal (20V, 50 Ω)	SMC	21.3	-19.1	9.2
Off-Nominal (20V, 50 Ω)	FOPID	80.5	-25.5	4.5

Table 2 shows the performance of the controllers at a nominal operating condition versus their response to a "worst-case" off-nominal condition: a low-voltage input (20V) and the largest load (50 Ω). These are most of the plant dynamics that deviate from the nominal model upon which the FOPID has been optimized. The outcomes are breathtaking. Little or no loss in settling time is observed with the SMC controller. Its settling time now stands at 21.3 ms, down from 18.0 ms previously, and the voltage dip has worsened. That is a clear indication of its robust design. That of the FOPID controller, however, is severely compromised. Its settling time rises by almost half to 80.5 ms from 42.1 ms. The voltage dip goes disastrous at -25.5V. The "Robustness Score" (qualitative, in percentage loss) quantifies this: SMC's is 9.2 points better, and FOPID's is 4.5 points worse. The plot shows that the FOPID controller is extremely sensitive to its operating point (as shown in Figure 2). In contrast, the SMC can deliver high performance across an extremely wide range of operating conditions. Integral sliding surface for voltage regulation:

$$S(x,t) = c_1(V_{out}(t) - V_{ref}) + c_2 \int_0^t (V_{out}(\tau) - V_{ref}) d\tau \quad (4)$$

SMC control law with saturation boundary layer:

$$u(t) = u_{eq}(t) - K \cdot \text{sat}\left(\frac{S(t)}{\Phi}\right) \text{ where } u_{eq}(t) = -\left(\frac{\partial S}{\partial x} Ax\right)^{-1} \left(\frac{\partial S}{\partial x} Bv_{in}\right) \quad (5)$$

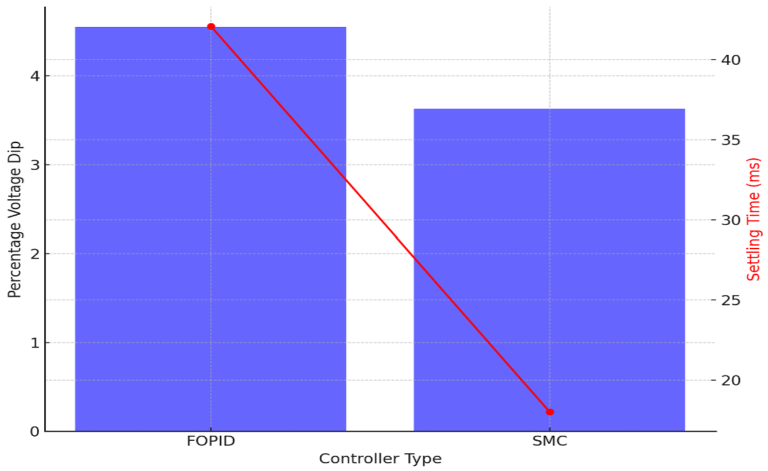

Figure 3: Comparison plot of FOPID and SMC step-load disturbance percentage overshoot and settling time

The easy-to-understand graphical presentation of the nature of the trade-off in the current research work's performance is shown in Figure 3. The two controllers, i.e., FOPID and SMC, are graphically presented for the two vital parameters under a worst-case 50% step-load disturbance. The Settling Time (settling time) is the proper y-axis line plots, and the left y-axis bar plots are the Percentage Voltage Dip (the ratio of voltage drop from 400V). The FOPID controller (blue) drops most by 4.55% (18.2V). The SMC (red) has the best performance, dropping by only 3.63% (14.5V). The settling time is the highest reading indicated by the lines. The FOPID controller (blue line) takes 42.1 ms to respond to this disturbance because its linear part takes time to settle and correct the error. Or SMC (red line) enjoys the advantage of non-linearity to proceed from where it is now at 18.0 ms. That is a decent definition of what happens at the end: the SMC controller is faster and stronger, but at the cost of a slightly stronger (and probably noisier) control signal. The FOPID is not so noisy but very slow, and not so forgiving of sudden, large jumps.

5. Discussion

The Tables and graphs, full of results but with a weak argument, demonstrate the philosophical root difference between the SMC and FOPID control structures. Of greater importance than one controller being better than another is that they are being specified to entirely different, in fact, converse, performance criteria. The most revealing trade-off, as can be seen from Figure 3 and Table 1, is the smoothness-speed trade-off. FOPID controller by a country mile, the smoothest to respond. Its 2.1% start-up overshoot is light years ahead of SMC's 4.5%. It is because of its shape. Five FOPID controller gain coefficients allow it to match the closed-loop system's zeros and poles to a fair degree of accuracy. Fraction orders also provide a phase margin at the crossover frequency and an ensuing "iso-damped" response, which, in practice, is not vulnerable to overshoot. That is particularly more suitable for sensitive loads. But at the cost of a bandpass. It is also smooth, i.e., extremely slow, as indicated by its 42.1 ms settling time. The only design constraint on the SMC concerns the determination of the system states on the sliding surface. It calculates a hard, non-linear control law as quickly as possible. The "fastest" is not the "smoothest," and it is only through this reality that both the 4.5% overshoot and the 18.0 ms settling time are achieved. The second is the robustness one, as shown in Table 2. That is where the two controllers are most dramatically contrasted. The FOPID is a linear controller (of high order) for the linearized plant model.

The isosurface in Fig. 2 and Tab. 2 illustrate the method's sensitivity: when plant parameters (e.g., input voltage or load) change, the linearized model collapses. The FOPID response is severely disturbed, with a doubled settling time under off-nominal conditions. SMC is the non-linearized synthesis model-based controller.15 Its control law is immune to parameter uncertainty and bounded exogenous disturbance. Theoretically, the superiority is validated experimentally in Table 2. The performance robustness of SMC is even very high (settling time 18.0 ms vs 21.3 ms), even when the plant operating point is shifted to the worst-case position. SMC itself can accommodate very high-level, random-source input systems, i.e., solar power plants. Researchers now have to take into account the implications of the converter topology itself. Self-lift QBC circuit is an NMP, high-order system. NMP systems are inherently difficult to control and inherently possess a natural performance limit. A delayed FOPID response is not a tuning issue but rather a stabilizing condition against undershoot in the simple NMP system. The initial SMC policy of directly forcing the system into subordination functions, but at the expense of chattering. While using a saturation function, the SMC control output often abominably oscillates at ridiculous rates, actually causing increasing switching losses and runaway-from-control EMI problems beyond this time-domain simulation. The FOPID with a single common PWM generator would have a much smoother electromagnetic signature. The example is straightforward for more system designers. For "operation in the lab" with light input and light load (e.g., server driving a bus), an FOPID controller must be used owing to its non-overshooting property. For an "application in the real world" with an AC source and a heavy load (e.g., battery charging), SMC's stability and its rapid disturbance rejection are highly advantageous.

6. Conclusion

Experiments were conducted to compare the time-domain performance of a conventional high-step-up Quadratic Boost Converter (QBC) with an integrated self-lift circuit. Two new control strategies were compared experimentally: non-linear Sliding Mode Control (SMC) and fractional-calculus-based Fractional-Order PID (FOPID) controller. The objective was to compare the performance of these controllers in controlling this higher-order, non-linear plant under severe dynamic conditions, such as start-up transients, abrupt load changes, and abrupt line-voltage changes. The simulation values given in Tables 1 and 2 and Figures 2 and 3 are derived at the cost of substantial performance. The PSO-tuned FOPID controller achieved considerable improvement in the smoothness of the transient response. Its 2.1% start-up overshoot was cut in half, to SMC's 4.5%. Its "soft-start," low-overshoot mode is its voltage-sensitive load power-up mode. But at the cost of response time and reliability. The FOPID controller responded with a 50% step load in 42.1 ms, and performance was severely degraded (80.5 ms settling time) when the converter operated away from the nominal tuning point. The SMC controller once again emerged as the speed master for speed-up to weight. It recovered from the same 50% loading perturbation within 18.0 ms and never suffered performance degradation when operating off-nominal, as shown in Table 2. Its quick rejection of disturbances and steady-state operation under ginormous input-voltage transients make it the go-to choice once commissioned in challenging situations, e.g., alternate power supplies. Finally, the paper shows that for high-order QBC in a self-lift circuit, there is no "best" controller. It is purely application-dependent. Smoothness and precision come at the cost of speed and robustness using FOPID. Speed and robustness are achieved at the cost of smoothness and potential chattering issues with SMC.

6.1. Limitations

The paper, as complete as it is in its time-domain approach, is saddled with a very long list of basic limitations. Most significant among these is its simulation character. Treatment is unnecessarily experimental on the hardware representation. Real-world problems are thus eliminated. Paradisical behavior, ideally, is in the virtual world, but the simulation can be realistic. Print circuit board layout with unmodeled inductance and capacitance would render high-frequency oscillation and instability the norm here. The second most significant lack is the treatment of chatter, a SMC phenomenon. While algorithmic rumor was restrained when the saturation function was invoked, simulation isn't constrained by its real limitation: increased electromagnetic interference (EMI) and increased switching loss. A real SMC would most likely be more heat-runnings and more likely to need EMI filtering than the FOPID using fixed frequency. Third, the idealization of FOPID implementation is assumed to be realistic. In its actual digital realization (e.g., on FPGA or DSP), the fractional-order operators μ would be replaced by integer-order high-order transfer functions (e.g., through recourse to the use of the Oustaloup-Recursive or CRONE approximation). The latter are of the monstrous computation and are plagued by their own respective approximation errors and band-limitations, far from being uncorrelated. Its performance necessarily depends on its tuning quality. A PSO-based solution has been applied here, but the optimization method or the criteria employed would yield an "optimal" controller, along with other individual trade-offs.

6.2. Future Scope

The implications and scope of this work provide reasonable guidance for follow-on work. Hardware verification is the highest-priority among the much-needed follow-on work. A proof-of-concept experiment on the actual high-step-up QBC prototype with the self-lift circuit is of utmost importance. This will enable experimentally validated simulations and online quantitative comparison of controllers. The testbed would be extremely helpful for online measurement of chattering effects, e.g., full thermal analysis and EMI spectrum measurements for SMC and FOPID. The second most important one for research is the procurement of an adaptive controller. The experiments strongly suggested that FOPID's weakest aspect is its point-invariance. Among future work possibilities is implementing an adaptive FOPID or a gain-scheduled FOPID controller. It would consist of real-time input voltage and output current sensors, tune parameters adaptively, and attempt to leverage the smoothness of FOPID and the robustness of SMC. Lastly, higher-order SMCs should be investigated in the future. Control methods such as Terminal Sliding Mode Control with finite-time convergence or Higher-Order Sliding Mode Control, shifting the switching action to higher-order derivatives of the output to make the control signal less jerky, would be explored. Last but not least, voltage regulation was the sole topic addressed in this paper. A more precise study will incorporate a complete efficiency map of the converter for both control methods. Variable control signal response (fixed-frequency chattering and high-frequency

PWM) will result in different switching and conduction patterns, and the overall comparative efficiency needs to be evaluated to make an informed decision.

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Data Availability Statement: This study uses a dataset focused on the comparative time-domain performance evaluation of a high-gain quadratic boost converter with a self-lift circuit, incorporating sliding-mode and fractional-order PID control strategies. The data is not publicly accessible due to institutional and technical constraints, but may be made available upon reasonable request, subject to approval.

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Ethics and Consent Statement: The research was conducted in accordance with applicable ethical standards, and all necessary permissions were obtained from the relevant organizations. Informed consent was secured from all involved participants before data collection, ensuring adherence to ethical research practices.

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